

Amendment
Serial No. 10/079,464
Attorney Docket No. 011703

AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes changes to Figs.1A - 4B, in which the figures are labeled "Prior Art".

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REMARKS

Claims 1-26 are pending. Claims 1, 6, 7 and 22 are amended.

Objection to the Drawings

The Examiner objects to Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A and 4B because they are described as being old in the art (see Specification pages 3-6) and they are missing a legend such as --Prior Art--. The drawings have been amended to overcome this objection.

Objection to the Claims

The Examiner objects to Claims 6 and 7. The claims have been amended to overcome the objection.

The Examiner's Rejection Under 35 U.S.C. § 102

Claim 22 was rejected under 35 U.S.C. § 102(e) as being anticipated by *Sochoux* (U.S. Patent 6,271,678). This rejection is respectfully traversed.

Sochoux discloses a printed circuit board having a termination device which includes a ferrite bead. The ferrite bead is combined with a resistor in a way as to provide resistance in series with the ferrite bead on a transmission line. The ferrite bead and resistor are packaged together in a single surface-mount package. The ferrite bead reduces electromagnetic interference.

The Examiner alleges that the ferrite magnetic material of *Sochoux* is an insulator. In addition, the Examiner alleges that *Sochoux* discloses doping the ferrite material with an insulative material. *Sochoux* states:

One embodiment [of] the present invention is implemented by configuring a ferrite bead to provide a substantial low-frequency resistance (such as by fabricating a ferrite bead having a constricted region **and/or doping with materials having less conductivity**) so that a single device provides both the high frequency impedance function of a typical ferrite bead and the low frequency resistance features desired.

(Col. 5, lines 17-26).

Sochoux does not disclose that material having less conductivity as being an insulator and it can be inferred that the ferrite bead is conductive based on the above disclosure.

The present invention relates to a method of terminating a bus for transmitting high frequency digital signals, and a wiring substrate having a chip type terminal resistor for terminating a bus. For example, to transmit digital signal of 1GHz, it is necessary to transmit high harmonic frequency components (as there are degrees of each high frequency component, up to around 10ghz must be considered) and apparent high harmonic frequency components associated with the transition time (about 5Ghz), together with a fundamental frequency component of the digital signal (1GHz).

The resistance of the terminal resistor provided at the terminal end is set to match the characteristic impedance of the bus. This avoids reflected waves from occurring. As a

consequence, when a terminal resistor may be considered as a pure resistance, there occurs substantially no problem of reflection.

However, the chip type terminal resistor, inevitably by its composition, has inductance (referred as L) and capacitance (referred as C). By the resonance of these L and C, high harmonic frequency components associated with the transition time are amplified. These amplified high frequency components cause the distortion to the pulse waveform of the high frequency digital signal being transmitted.

In the present invention, on the bus from the start terminal to the end terminal, the high frequency digital signal with only little distortion to the pulse waveform is transmitted. Therefore, on the bus, the digital signal including high harmonic frequency components, apparent high frequency components associated with the transition time is transmitted and the base frequency component.

The digital signal arriving at the terminal end of the bus then ends its role. Consequently, in the present invention, the terminal end of the bus is terminated, for absorbing the energy by the digital signal or by the resonance of LC of the chip type terminal resistor.

In contrast, Sochoux relates to a source terminator device, in which a signal is transmitted from source to load via a transmission line.

Between the source and the transmission line, a source terminator device is provided.

This source terminator device is composed of a resistor and a ferrite bead serially connected.

By providing this source terminator device, EMI (electromagnetic interference) from the transmission line is decreased. The decrease of the EMI allows high frequency components to be suppressed.

In Sochoux, in order to decrease the EMI from the transmission line, high frequency components are suppressed by the source terminator device.

As described above, in Sochoux, high frequency components included in the transmitted signal are suppressed. Then, when the signal is a clock, the waveform of the clock gets distortion.

On the contrary, in the present invention, while all the frequency components (high frequency component energy including base frequency components of the digital signal, high harmonic frequency components of the digital signal, high harmonic frequency components, and apparent high frequency components associated with the transition time) are transmitted on the bus, their decrease is limited at the minimum amount. The EMI possibly occurred from the bus is not considered.

Further, the digital signal arriving at the terminal end of the bus does not occur a reflection. Therefore, the digital signal transmitted from the start terminal to the end terminal on the bus is not distorted.

As explained above, the basic ideas of Sochoux and the invention are different.

The Examiner's Rejection Under 35 U.S.C. § 103

Claims 1, 13 and 14 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Otsuka et al.* (JP 2000174505) in view of Sochoux; and Claims 1-2, 6-8 and 13-15 under 35 U.S.C. 103(a) as being unpatentable over *Otsuka et al.* in view of *Fukaya* (US Patent 5,955,938). Favorable reconsideration of these rejections is respectfully requested.

Otsuka et al. discloses paired transmission lines having a terminal resistor on one end. The Examiner admits that *Otsuka et al.* does not teach that (1) the terminal resistor is provided with an insulator having a larger dielectric loss angle than the substrate as recited in Claims 1, 6, 7 and 13; (2) the resistor is a chip as recited in Claims 6, 7 and 13; (3) the transmission lines are multiple pairs, each pair having a termination as recited in Claims 6 and 7; (4) the insulator includes glass containing a modified ionized additive as recited in Claim 2; (5) the insulator covers the resistor as recited in Claims 6 and 7; and (6) the insulator is a mixture of glass, resin and ionized additive as recited in Claims 8 and 15.

In the present invention, dielectric loss angle of the substrate is preferably small, in order to limit the decrease at the minimum amount while transmitting all the frequency components included in the digital signal. Further, an insulator around or in the vicinity of the terminal resistor preferably has a large dielectric loss angle. So, in the present invention, for the insulator of the terminal resistor, "an insulator having larger dielectric loss angle at least in the frequency region of the digital signal than the insulative substrate" is used.

This idea is not taught either in *Otsuka et al.*, or in Sochoux.

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It is respectfully submitted that the features of the amended claims are not taught or suggested by the cited art.

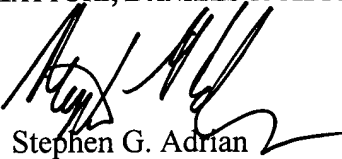
An Information Disclosure statement is filed herewith. The Examiner is requested to acknowledge consideration of the cited references in the next communication.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,
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Attachments: Replacement Sheets
Information Disclosure Statement